RISC-V Instruction Set Summary

TABLE 1 - RV32I: RISC-V Integer instructions

op	Func3	Func7	Type	Instruction	Description	Operation
0000011(3)	000	-	I	lb rd, imm(rs1)	Load byte	Rd = SignExt([Address]$_{7:0}$)
0000011(3)	001					
0000011(3)	010					
0000011(3)	100					
0000011(3)	101					
0010011(19)	000					
0010011(19)	001					
0010011(19)	010					
0010011(19)	011	0000000		sltiu rd, rs1, imm	Set less than imm. unsigned	Rd = (rs1 < SignExt(imm))
0010011(19)	100					
0010011(19)	101	0000000		srli rd, rs1, uimm	Shift right logical immediate	Rd = rs1 >> uimm
0010011(19)	101	0100000				
0010011(19)	110					
0010011(19)	111					
0010111(23)	-					
0100011(35)						
0100011(35)						
0100011(35)						
0110011(51)	000					
0110011(51)	001					
0110011(51)	010					
0110011(51)	011					
0110011(51)	100					
0110011(51)	101					
0110011(51)	101					
0110011(51)	110					
0110011(51)	111					
0110111(55)						
1100011(99)						
1100011(99)						
1100011(99)						
1101111(111)						